In re Patent Application of:
CAPPELLETTI
Serial No. **Not Yet Assigned**
Filing Date: **Herewith**
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In the Claims:

Claims 1-19 (CANCELLED)

Please add new claims 20-23 as follows:

20. (NEW) A method for making a floating gate transistor for a memory cell of a non-volatile memory on a semiconductor substrate, the method comprising the steps of:

forming a gate oxide layer on the substrate and forming a floating gate region on the gate oxide layer by forming a first layer of material of a first type adjacent to the surface of the semiconductor substrate and forming a second layer of material of a second type whose electron affinity lies intermediate to those of the first layer and the floating gate region for developing a first potential barrier between the semiconductor substrate and the gate oxide layer and for developing a second different potential barrier between the floating gate region and the gate oxide layer.

21. A method according to Claim 20, and further comprising the step of forming the second layer as a silicon nitride layer.

22. A method according to Claim 20, and further comprising the step of forming the second layer at a thickness less than a thickness of said first layer.

23. A method according to Claim 20, and further comprising the step of depositing the second layer at a low temperature.